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1. (Original) A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to one of the source and drain regions;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

2. (Original) The memory of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer separating the polysilicon floating gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

3. (Original) The memory of claim 1, wherein the control gate includes a polysilicon control gate having a metal layer separating the polysilicon control gate and the metal oxide insulator, the metal layer in contact with the metal oxide insulator.

4. (Original) The memory of claim 1, wherein the gate oxide includes silicon dioxide having a tunnel barrier height of about 3.2 eV.

5. (Original) The memory of claim 1, wherein the metal oxide insulator includes a transition metal oxide.

6. (Original) The memory of claim 1, wherein the metal oxide insulator includes aluminum oxide.

7. (Original) The memory of claim 1, wherein the metal oxide insulator includes lead oxide.

8. (Original) The memory of claim 1, wherein the metal oxide insulator includes zirconium oxide.

9. (Original) The memory of claim 1, wherein the metal oxide insulator includes titanium oxide.

10. (Original) The memory of claim 1, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

11. (Original) The memory of claim 1, wherein the channel region includes an n-type channel.

12. (Original) A memory comprising: a memory cell, the memory cell including

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide having a first tunneling barrier height;

a control gate opposing the floating gate;

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a second tunneling barrier height, the second tunneling barrier height being less than the first tunneling barrier height;

a first metal layer separating the metal oxide insulator and the floating gate, the first metal layer in contact with the floating gate;

a second metal layer separating the metal oxide insulator and the control gate, the metal layer in contact with the control gate, wherein the memory is adapted to operate the memory cell in a volatile memory mode and in a non-volatile memory mode.

13. (Original) The memory of claim 12, wherein the control gate is a vertical control gate.

14. (Original) The memory of claim 13, wherein the control gate is a polysilicon edge defined vertical control gate.

15. (Original) The memory of claim 12, wherein the memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

16. (Original) The memory of claim 12, wherein the metal oxide insulator includes a transition metal oxide.

17. (Original) The memory of claim 12, wherein the metal oxide insulator includes aluminum oxide.

18. (Original) The memory of claim 12, wherein the metal oxide insulator includes niobium oxide.

19. (Original) The memory of claim 12, wherein the metal oxide insulator includes tantalum oxide.

20. (Original) The memory of claim 12, wherein the floating gate includes a horizontally oriented floating gate in contact with the gate oxide.

21. (Original) The memory of claim 12, wherein the gate oxide includes silicon oxide having a tunneling barrier height of about 3.2 eV, the floating gate includes polysilicon, and the control gate includes polysilicon.

22. (Original) A memory comprising:

an array of memory cells, each memory cell including:

a source region and a drain region separated by a channel region in a substrate;

a storage capacitor coupled to the drain region;

a floating gate opposing the channel region;

a gate oxide separating the floating gate from the channel region, the gate oxide including silicon oxide having a tunneling barrier height of about 3.2 eV;

a control gate opposing the floating gate; and

a metal oxide insulator separating the control gate from the floating gate, the metal oxide insulator having a tunneling barrier height less than the tunneling barrier height of the silicon oxide;

a number of bit lines coupled to the source regions along a first direction in the array of memory cells; and

a number of word lines coupled to the control gates along a second direction in the array of memory cells, wherein the memory is adapted to operate each memory cell in the array of memory cells in a volatile memory mode and in a non-volatile memory mode.

23. (Original) The memory of claim 22, wherein each memory cell is controllable to access a first charge representing a data value from the storage capacitor in the volatile memory mode and a second charge representing a data value from the floating gate in the non-volatile memory mode such that the first charge is accessible without affecting the second charge and the second charge is accessible without affecting the first charge.

24. (Original) The memory of claim 22, wherein each memory cell further includes a first metal layer separating the floating gate and the metal oxide insulator, the first metal layer in

contact with the metal oxide insulator, and a second metal layer separating the control gate and the metal oxide insulator, the second metal layer in contact with the metal oxide insulator.

25. (Original) The memory of claim 24, wherein the floating gate includes polysilicon, the first metal layer contacting the floating gate, and the control gate includes polysilicon, the second metal layer contacting the control gate.

26. (Original) The memory of claim 25, wherein the metal oxide insulator includes a metal oxide insulator having a tunneling barrier height of less than 2 eV.

27. (Original) The memory of claim 26, wherein the control gate is a polysilicon edge defined vertical control gate.

28. (Original) The memory of claim 25, wherein the metal oxide insulator includes a transition metal oxide.

29. (Original) The memory of claim 25, wherein the metal oxide insulator includes aluminum oxide.

30. (Original) The memory of claim 25, wherein the metal oxide insulator includes lead oxide.

31. (Original) The memory of claim 25, wherein the metal oxide insulator includes zirconium oxide.

32. (Original) The memory of claim 25, wherein the metal oxide insulator includes niobium oxide.

33. (Original) The memory of claim 25, wherein the metal oxide insulator includes tantalum oxide.

34. (Original) The memory of claim 25, wherein the metal oxide insulator includes titanium oxide.

35. (Original) The memory of claim 25, wherein the metal oxide insulator includes a Perovskite metal oxide insulator.

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